Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.102”**

**GATE**

**SOURCE**

**.106”**

**Top Material: Al**

**Backside Material: Ni Ag**

**Bond Pad Size: Gate .015” X .021”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .102” X .106” DATE: 8/25/21**

**MFG: FAIRCHILD THICKNESS .016” P/N: SFRU9130**

**DG 10.1.2**

#### Rev B, 7/19/02